

Ethernet and its principles



Ethernet beginnings are somewhere between 1968-1972, when the ALOHA network was being developed in Hawaii. On this radio-based network, several principles later used in the Ethernet were tested. One of the main ones involves sharing of a single medium by several stations using a time multiplex with random timing. Whenever a station needed to send a packet, it would transmit it and wait for acknowledgement. If the packet was not acknowledged within a specified time (perhaps due to a collision -- several stations trying to transmit at the same time), it was re-transmitted after a random delay. During 1972-1977, Xerox company followed up on this work in its research center (PARC). Another main principle of Ethernet, carrier sensing, originated here. Before a station can transmit, it has to monitor the medium for a given period, and only begin transmission if no one else transmits. Both principles were embedded into the title of the patent that expressed the first definition of Ethernet -- "Carrier-Sense Media Access with Collision Detection" -- CSMA/CD. The first experimental network connected computers called ALTO with the first laser printers named EARS. Its transmission speed of 2,94Mbps was derived from ALTO's system clock.

These beginnings gave Ethernet its relative reliability based on several robust properties. First, synchronization is transmitted at the beginning of each frame. Ethernet utilizes a shared medium and serial communication. Communication occurs in frames. Each frame starts with a 6-byte destination address, followed by a 6-byte source address, actual data, and ends with a 4-byte CRC. A synchronization sequence is transmitted before each frame; it consists of 31 pairs of '0' and '1' bits followed by two '1' bits that indicate the beginning of a frame. These 64 bits are used for synchronization and automatic adjustment of receiver gains. Ethernet adapters insert them automatically when transmitting and strip them when receiving. (Note: A receiver does not have to receive all 64 bits every time. Some of them may be lost if the transmitter does not turn on fast enough or if the receiver gain is not initialized properly.)

Second, each data bit is transmitted together with a synchronization bit. This is implied by modulation -- Ethernet uses so-called Manchester II. This modulation scheme splits each bit interval into halves. The inverse of the data bit is transmitted in the first half, and its direct value in the second half. It is possible to say that each bit coming to the transmitter is replaced by two bits, each occupies half of the original time slot. '0' is replaced by '10', '1' is replaced by '01'. For example, the above synchronization sequence should look like this:



Clock signal on the first line synchronizes is input into the transmitter only. The receiver has to reconstruct the clock from the incoming data with a phase lock. Second line shows the data as sent by the Ethernet controller core into the modulator. Third line shows the data as they are sent into the medium by the modulator.

A more detailed look at the transmitted data reveals another important property of this modulation -- DC level remains constant during transmission. This solves two problems: first, it makes it easy to electrically isolate link circuitry from the host computer. All signals are symmetrized (to remove the DC component) and then isolated by transformers. Second, if symmetrization is not applied, it is possible to measure the average level of this DC component. Average value is monitored during transmission, and if a deviation is detected (most often caused by simultaneous transmission of several stations), collision is signalled. Such a collision detection is used for example in the MAU circuitry for the coaxial cable.

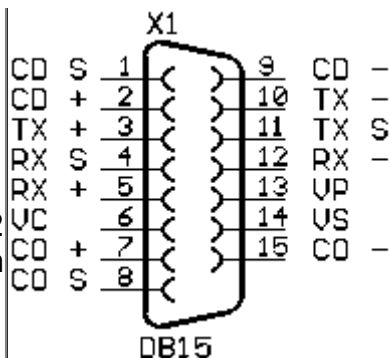
So, what does data transmission over e.g. a coaxial cable look like? Transmitted data as well as other signals (received data, collision signalization, power) pass through isolation circuitry into MAU (Media Attachment Unit). MAU circuitry may be implemented directly onboard or as a separate "box" attached to standard AUI interface connector.



AUI Connector



AUI connector is a DB15 connector (2 rows, trapezoidal Cannon, 8+7 pins). Pin assignment is detailed in the following table:



Pin	IEEE name	Pair	Description	Direction
3	DO + (Data Out +)	Transmit	TX +	DTE->MAU
10	DO - (Data Out -)		TX -	DTE->MAU
11	DO S (Data Out Shield)		TX S	DTE->MAU
5	DI + (Data In +)	Receive	RX +	DTE<-MAU
12	DI - (Data In -)		RX -	DTE<-MAU
4	DI S (Data In Shield)		RX S	DTE->MAU
7	CO + (Control Out +)	Optional		DTE->MAU
15	CO - (Control Out -)			DTE->MAU
8	CO S (Control Out Shield)			DTE->MAU
2	CI + (Control In +)	Collision	CD +	DTE<-MAU
9	CI - (Control In -)		CD -	DTE<-MAU
1	CI S (Control In Shield)		CD S	DTE->MAU
6	VC (Voltage Common)	Power		DTE->MAU
13	VP (Voltage Plus)			DTE->MAU
14	VS (Voltage Shield)			DTE->MAU

where DTE->MAU indicates direction from the device into the medium.

- ▶ [CTI - Coaxial Transceiver Interface](#)
- ▶ [TPEX - Twisted Pair Ethernet Transceiver](#)
- ▶ [FL MAU - Fiber optic Link Medium Attachment Unit](#)

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